

**What is claimed is:**

- 1 1. A semiconductor chip having circuitry, the semiconductor chip comprising:  
2 a metal bond pad over the circuitry and insulated on at least two sides by  
3 passivation material;  
4 a diffusion barrier layer over the metal bond pad; and  
5 a metal layer over the circuitry, the metal bond pad, the diffusion barrier layer,  
6 and at least partially over the passivation material, the metal layer being configured and  
7 arranged for connecting to a wire bond and the diffusion barrier layer being constructed  
8 and arranged to mitigate inter-metallic compounds forming as a reaction to the metal  
9 layer connecting to the wire bond.
- 1 2. The semiconductor chip of claim 1, wherein the diffusion barrier layer includes  
2 TiN.
- 1 3. The semiconductor chip of claim 2, wherein the diffusion barrier layer has a  
2 thickness that is at least 0.5 micron.
- 1 4. The semiconductor chip of claim 2, wherein the diffusion barrier layer has a  
2 thickness that is at least 1.0 micron.
- 1 5. The semiconductor chip of claim 1, wherein the semiconductor chip is  
2 configured and arranged as a flip chip.

1 6. The semiconductor chip of claim 1, wherein the metal bond pad includes  
2 aluminum.

1 7. The semiconductor chip of claim 6, wherein the diffusion barrier layer includes  
2 TiN.

1 8. The semiconductor chip of claim 7, wherein the diffusion barrier layer is further  
2 constructed and arranged to mitigate inter-metallic Al/Au compounds forming as a  
3 reaction to the metal layer connecting to the wire bond.

1 9. The semiconductor chip of claim 8, wherein the diffusion barrier layer has a  
2 thickness that is at least 0.5 micron, and the metal layer has a thickness that is at least 3  
3 microns.

1 10. The semiconductor chip of claim 1, wherein the metal bond pad and the metal  
2 layer include the same type of metal.

1 11. A semiconductor chip having circuitry, the semiconductor chip comprising:  
2 an aluminum bond pad over the circuitry and insulated on at least two sides by  
3 passivation material;  
4 a diffusion barrier layer, including TiN, over the aluminum bond pad; and  
5 a metal layer over the circuitry, the metal bond pad, the diffusion barrier layer,  
6 and at least partially over the passivation material, the metal layer being configured and

7 arranged for connecting to a wire bond and the diffusion barrier layer being constructed  
8 and arranged to mitigate inter-metallic aluminum-based compounds forming as a  
9 reaction to the metal layer connecting to the wire bond.

1 12. The semiconductor chip of claim 8, wherein the diffusion barrier layer has a  
2 thickness that is at least 0.5 micron, the metal layer has a thickness that is at least 3  
3 microns.

1 13. The semiconductor chip of claim 12, wherein the diffusion barrier layer is  
2 further constructed and arranged to mitigate inter-metallic Al/Au compounds forming as  
3 a reaction to the metal layer connecting to the wire bond.

1 14. A semiconductor chip having circuitry, the semiconductor chip comprising:  
2 an aluminum bond pad over the circuitry and insulated on at least two sides by  
3 means for electrically insulating the aluminum bond pad;  
4 barrier means, including TiN, over the aluminum bond pad; and  
5 a metal layer over the circuitry, the metal bond pad, the barrier means, and at  
6 least partially over the means for electrically insulating the aluminum bond pad, the  
7 metal layer being configured and arranged for connecting to a wire bond and the barrier  
8 means for mitigating inter-metallic aluminum-based compounds forming as a reaction  
9 to the metal layer connecting to the wire bond.